REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-4, 8-10, and 14-32 are pending in this application. Claims 1-4, 10, 16, 17, 18, and 19 are amended, Claims 5-7 and 11-13 are canceled without prejudice, and Claims 24-32 are added by the present amendment.

In the outstanding Office Action, the specification was objected to; the drawings were objected to; the title was objected to; Claims 1, 10, and 16 were rejected under 35 U.S.C. §112, first paragraph; and Claims 1, 10, and 16 were rejected under 35 U.S.C. § 112, second paragraph.

Regarding the objections to the specification and the title, the specification has been amended to recite that a voltage of a bit line side select gate line SGD is changed from Vdd+α to Vdd and to better conform with U.S. patent practice. The amendments to the specification find support for example in Figure 8 and the description of the second embodiment. No new matter is believed to be added. Further, the title has been amended to be more descriptive of the invention to which the claims are directed. Accordingly, it is respectfully requested that these objections be withdrawn.

Regarding the objection to the drawings, Figure 3 is amended to show voltages Vpre and Vdd+α, which finds support in the specification for example at page 14, lines 16-19, and at page 14, lines 19-20. No new matter is believed to be added. A formal drawing including amended Figure 3 is submitted with this response. Accordingly, it is respectfully requested that this objection be withdrawn.

Regarding the rejections of Claims 1, 10, and 16 under 35 U.S.C. § 112, first and second paragraphs, independent Claims 1, 10, and 16 have been amended to more clearly

recite relationships among various memory transistors and to clarify a connection of a NAND cell to a bit line and a common source line. Claims 2-4 and 17-19 have been amended to be consistent with independent Claims 1 and 16. The claim amendments find support for example in Figures 3, 6, and 9, which show the features of independent Claims 1, 10, and 16, respectively. No new matter is believed to be added. Accordingly, it is respectfully requested that these rejections be withdrawn.

In an effort to expedite the prosecution of this application and to promote a better understanding of the present invention, elements of a semiconductor device of independent Claim 1 are listed below based on Figure 3, which is only a non-limiting example. In this non-limiting example, Figure 3 shows a plurality of memory transistors MC00-MC150, a bit line BLO, a first select gate transistor SG10, a common source line SL, a second select gate transistor SG20, a second memory transistor counted from the bit line side is MC10, a write voltage Vpgm, a reference voltage OV, a third memory transistor counted from the bit line side is MC20, a medium voltage Vpass, a first memory transistor counted from the bit line side is MC00, and the remaining memory transistors are MC30 to MC150.

New Claims 24-32 have been added to set forth the invention in a varying scope and Applicants submit the new claims are supported by the originally filed specification. More specifically, Claims 24-32 find support for example in Figure 7. No new matter is believed to be added. Accordingly, it is respectfully submitted that new Claims 24-32 are also in condition for allowance.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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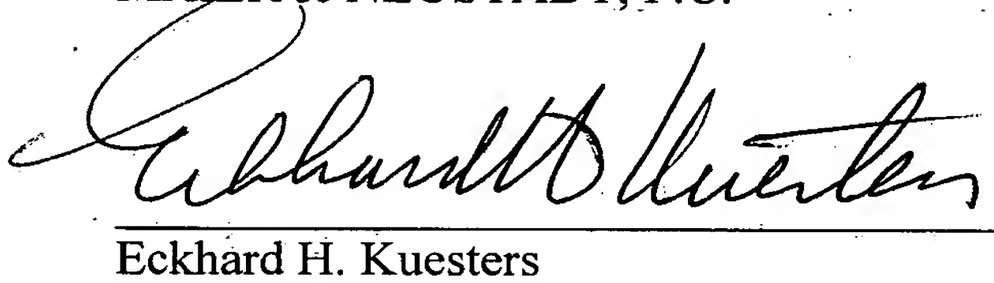

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